What is claimed is:

1. A method of manufacturing a semiconductor integrated circuit device, comprising: (a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a second major surface side of a mask substrate, said mask substrate having on a first major surface thereof a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern; and (b) the step of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby said integrated circuit pattern is imaged on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer and thus transferred.

2. The method of manufacturing a semiconductor integrated circuit device according to Claim 1, wherein the wavelength of said exposure light is at least 100 nm less than 250 nm.

3. The method of manufacturing a semiconductor integrated circuit device according to Claim 2, wherein said wavelength of said exposure light is at least 100 nm but less than 200 nm.

4. The method of manufacturing a semiconductor integrated circuit device according to Claim 3,

wherein, in the peripheral portion of the first major surface of said mask substrate, a light screening metal region is provided.

5. The method of manufacturing a semiconductor integrated circuit device according to Claim 4, wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

6. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface or a second major surface side of said mask substrate in the state in which the peripheral region of said mask substrate is held on a mask holding mechanism, said mask substrate having on the first major surface thereof a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern, said resist pattern being not provided on said peripheral region; and

(b) the step of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby said integrated circuit pattern is imaged on a photo resist

film formed on a first major surface of a semiconductor integrated circuit wafer and thus transferred.

7. The method of manufacturing a semiconductor integrated circuit according to Claim 6, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

8. The method of manufacturing a semiconductor integrated circuit according to Claim 7, wherein, wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

9. The method of manufacturing a semiconductor integrated circuit device according to Claim 8, wherein, in the peripheral portion of the first major surface of said mask substrate, a light screening metal region is provided.

10. The method of manufacturing a semiconductor integrated circuit device according to Claim 9, wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

11. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum

ultraviolet exposure light from a first major surface or second major surface side of a mask substrate, said mask substrate having, in an integrated circuit pattern region of the first major surface thereof, a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern and having a light screening metal region provided in the peripheral region of said first major surface; and (b) the step of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

12. The method of manufacturing a semiconductor integrated circuit device according to Claim 11, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

13. The method of manufacturing a semiconductor integrated circuit device according to Claim 12, wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

14. The method of manufacturing a semiconductor integrated circuit device according to Claim 13,

wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

15. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface or a second major surface side of a mask substrate, said mask substrate having, in an integrated circuit pattern region of the first major surface thereof, a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern, wherein a pellicle is contact-fixed in that part of the peripheral portion of said integrated circuit pattern region in which said photo resist pattern is not formed; and

(b) the step of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

16. The method of manufacturing a semiconductor

integrated circuit device according to Claim 15, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

17. The method of manufacturing a semiconductor integrated circuit device according to Claim 16, wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

18. The method of manufacturing a semiconductor integrated circuit device according to Claim 17, wherein, in the peripheral portion of the first major surface of said mask substrate, a light screening metal region is provided.

19. The method of manufacturing a semiconductor integrated circuit device according to Claim 18, wherein, on the first major surface of said mask substrate, said pellicle is contact-fixed on said light screening metal region.

20. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface side or a second major surface side of a mask substrate, said mask substrate having, on the first major surface thereof, a halftone light shielding pattern comprising a photo resist pattern which

constitutes an integrated circuit pattern on a mask; and

(b) the step of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

21. The method of manufacturing a semiconductor integrated circuit device according to Claim 20, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

22. The method of manufacturing a semiconductor integrated circuit device according to Claim 21, wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

23. The method of manufacturing a semiconductor integrated circuit device according to Claim 22, wherein, in the peripheral portion of the first major surface of said mask substrate, a light screening metal region is provided.

24. The method of manufacturing a semiconductor integrated circuit device according to Claim 23, wherein, on the first major surface of said mask

substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening region.

25. A method of manufacturing a semiconductor integrated circuit device, comprising:
(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface side or a second major surface side of a mask substrate, which has, on the first major surface thereof, a light shielding pattern which is an integrated circuit pattern on a Lebenson type phase shift mask and comprises a photo resist pattern; and
(b) the step of reduction-projecting, by a projection optical system, the exposure light which has transmitted through said mask substrate, whereby, on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

26. The method of manufacturing a semiconductor integrated circuit device according to Claim 25, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

27. The method of manufacturing a semiconductor integrated circuit device according to Claim 26, wherein, wherein the wavelength of said exposure light

is at least 100 nm but less than 200 nm.

28. The method of manufacturing a semiconductor integrated circuit device according to Claim 27, wherein, in the peripheral portion of said first major surface, a light screening metal region is provided.

29. The method of manufacturing a semiconductor integrated circuit device according to Claim 28, wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

30. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface or a second major surface side of a mask substrate, said mask substrate having, in an integrated circuit pattern region of said first major surface thereof, a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern, wherein a pellicle is contact-fixed in the peripheral portion of said integrated circuit pattern of said first major surface so as to cover said integrated circuit pattern; and

(b) the step of reduction-projecting, by a projection

optical system, said exposure light which has transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit, said integrated circuit pattern is imaged and thus transferred.

31. The method of manufacturing a semiconductor integrated circuit device according to Claim 30, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

32. The method of manufacturing a semiconductor integrated circuit device according to Claim 31, wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

33. The method of manufacturing a semiconductor integrated circuit device according to Claim 32, wherein, in the peripheral portion of the first major surface of said mask substrate, a light screening metal region is provided.

34. The method of manufacturing a semiconductor integrated circuit device according to Claim 33, wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

35. A method of manufacturing a semiconductor

integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface or a second major surface side of a mask substrate, said mask substrate having, in an integrated circuit pattern region of said first major surface thereof, a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern, wherein a protective film is formed on said photo resist pattern so as to cover said integrated circuit pattern region of said first major surface; and

(b) the step of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

36. The method of manufacturing a semiconductor integrated circuit device according to Claim 35, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

37. The method of manufacturing a semiconductor integrated circuit device according to Claim 36,

wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.